What is claimed is:

1. A reconfigurable processor for processing digital logic functions, comprising:

a microcontroller; and

a plurality of processing elements,

wherein the plurality of processing elements are arranged in one or more pipeline stages each comprising one or more processing elements, and

wherein the microcontroller executes a program comprising:

configuring the plurality of processing elements by sending configuration information to the plurality of processing elements,

determining whether data has been processed by the one or more processing elements of a pipeline stage, and

if data has been processed by the one or more processing elements of the pipeline stage, reconfiguring at least one of the one or more processing elements of a pipeline stage to define a subsequent pipeline stage.

2. The processor of claim 1 further comprising one or more decoders connected to the microcontroller, wherein each decoder is connected to one or more of the plurality of processing elements.

3. The processor of claim 2 further comprising one or more global interconnection busses used to connect the plurality of processing elements to the one or more decoders.

4. The processor of claim 2 wherein reconfiguring the plurality of processing elements is performed via the one or more decoders.

5. The processor of claim 1 further comprising a plurality of local interconnection busses.

6. The processor of claim 5 wherein each processing element is connected to one or more other processing elements by one or more of the local interconnection busses.

7. The processor of claim 6 wherein the plurality of processing elements are interconnected in a toroidal interconnect structure.

8. The processor of claim 1 wherein the microcontroller is in communication with a memory, and the program is stored in the memory.

9. The processor of claim 1 wherein the microcontroller is an off-chip device.

10. A method of dynamically reconfiguring a pipelined instruction set processor comprising:

configuring a plurality of pipeline stages by a microcontroller, wherein each pipeline stage includes one or more processing elements;

processing data through one or more of the plurality of pipeline stages;

reconfiguring, by the microcontroller, at least one of the one or more pipelined stages to define at least one subsequent pipeline stage; and

routing processed data through the at least one reconfigured pipeline stage.

11. The method of claim 10 wherein the reconfiguring step is performed while the processed data is further processed by the plurality of pipelined stages.

12. A reconfigurable processor for processing digital logic functions, comprising:

an on-chip microcontroller; and

a plurality of processing elements,

wherein the plurality of processing elements are arranged in one or more pipeline stages each comprising one or more processing elements, and

wherein the microcontroller executes a program comprising:

configuring the plurality of processing elements by sending configuration information to the plurality of processing elements,

determining whether data has been processed by the one or more processing elements of a pipeline stage, and

if data has been processed by the one or more processing elements of the pipeline stage, reconfiguring at least one of the one or more processing elements of a pipeline stage to define a subsequent pipeline stage.

13. The processor of claim 12 further comprising one or more decoders connected to the microcontroller, wherein each decoder is connected to one or more of the plurality of processing elements.

14. The processor of claim 13 further comprising one or more global interconnection busses used to connect the plurality of processing elements to the one or more decoders.

15. The processor of claim 13 wherein configuring the plurality of processing elements is performed via the one or more decoders.

16. The processor of claim 12 further comprising a plurality of local interconnection busses.

17. The processor of claim 16 wherein each processing element is connected to one or more other processing elements by one or more of the local interconnection busses.

18. The processor of claim 17 wherein the plurality of processing elements are interconnected in a toroidal interconnect structure.

19. The processor of claim 12 wherein the microcontroller is in communication with a memory, and the program is stored in the memory.